UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,011	05/14/2001	Martin J. Ratcliffe	00-323 1496.00121	1191

7590 07/01/2005

Intellectual Property Law Department
LSI Logic Corporation
M/S D-106
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER	
ROSARIO, DENNIS	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,011	RATCLIFFE, MARTIN J.	
	Examiner	Art Unit	
	Dennis Rosario	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment was received on March 2, 2005. Claims 1-23 are pending.

Response to Arguments

2. Applicant's arguments, see amendment, page 10, last three lines, "...Cahill does not disclose or suggest **A** finite state machine configured to **allow multiple luma AND multiple chroma** picture requests to follow in sequence...", filed 3/2/2005, with respect to the rejection(s)of claim(s) 1,15 and 16 under Cahill, III et al. (US Patent 5,784,047 A) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yasuki et al. (US Patent 5,712,689 A) in view of Cahill, III et al. (US Patent 5,784,047 A).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2,4-16 and18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuki et al. (US Patent 5,712,689 A) in view of Cahill, III et al. (US Patent 5,784,047 A).

Regarding claim 1, Yasuki et al. teaches an apparatus for variably scaling video picture signals comprising:

a) a first circuit (Fig. 12, num. 332 is a circuit.) configured to generate one or more data signals (Fig. 12, num. 332 is a circuit configured to generate data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459.) vertically scaled (Fig. 12, num. 332 is a circuit configured to generate data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 as a scaled data signal using "compression or expansion" in col. 13, lines 1,2.) to a first value (Fig. 12, num. 332 is a circuit configured to generate data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 as a scaled data signal using "compression or expansion" in col. 13, lines 1,2 to a first value of "2/3" in col. 6, line 32.) in response to

(i) said video picture signals (Fig. 12, num. 332 is a circuit configured to generate data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 as a scaled data signal using "compression or expansion" in col. 13, lines 1,2 to a first value of "2/3" in col. 6, line 32 in response to said video picture signals "Y", "C" as shown inputted to numeral 332 of fig. 12.) and

(ii) one or more first control signals (Fig. 12, num. 332 is a circuit configured to generate data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 as a scaled data signal using "compression or expansion" in col. 13, lines 1,2 to a first value of "2/3" in col. 6, line 32 in response to said video picture signals "Y", "C" as shown inputted to numeral 332 of fig. 12 and one first control signal or arrow that corresponds to a BUS CONTROLLER of fig. 12,num. 338 between numerals 332 and 338.);

b) a second circuit (Fig. 12, num. 334 is a second circuit.) configured to generate one or more output signals (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335.) horizontally scaled (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 scaled via "compres-sion or expansion" in col. 13, lines 26,27.) to a second value (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 scaled via "compres-sion or expansion" in col. 13, lines 26,27 to a second value or "predetermined size" in col. 13, line 35.) in response to said one or more data signals (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 scaled via "compression or expansion" in col. 13, lines 26,27 to a second value or "predetermined size" in col. 13, line 35 in response to said data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 which is inputted to fig. 12,num. 334.) and said one or more first control signals (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 scaled via "compression or expansion" in col. 13, lines 26,27 to a second value or "predetermined size" in col. 13, line 35 in response to said data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 which is inputted to fig. 12,num. 334 and said more first control signals or arrow between numerals 338 and 459. Note that the arrow corresponds to fig. 12,num. 338: BUS CONTROLLER; thus the arrow can be called a control arrow.), wherein said first value ("2/3" in col. 6, line 32)...

...and said second value ("predetermined size" in col. 13, line 35) are independently selectable (or "perform the compression/expansion processing flexibly" in col. 1, lines 62,64) and

c) an address generator circuit (Fig. 5,num. 384: DMA is a circuit that generates an ADDRESS LINE as shown in fig. 5.) configured to generate said one or more first control signals (Fig. 5,num. 384: DMA is a circuit that generates an ADDRESS LINE as shown in fig. 5 configured with multiple outputs, DATA LINE,CS, to generate said one or more first control signals outputted from fig. 12, num. 338 to numerals 332 and 334.), wherein said address generator (Fig. 5,num. 384: DMA) comprises:

a finite state machine (Fig. 5,num. 385: STATE MACHINE) configured to allow multiple luma and multiple chroma picture requests (Fig. 5,num. 385: STATE MACHINE configured as shown in fig. 12, num. 338: BUS CONTROLLER to allow multiple luma, as shown in figure 12, label "Y" inputted to numerals 332,322,325 and multiple chroma, as shown in fig. 12, label "C" inputted to numerals 332,322,325, picture requests, REQ and IREQ 1, BUS-REQ...)...

...to follow in sequence (Fig. 5,num. 385: STATE MACHINE configured as shown in fig. 12, num. 338: BUS CONTROLLER to allow multiple luma, as shown in figure 12, label "Y" inputted to numerals 332,322,325 and multiple chroma, as shown in fig. 12, label "C" inputted to numerals 332,322,325, picture requests, REQ and IREQ 1, BUS-REQ to follow in sequence via a switch 459 of fig. 12 that selects luma Y of fig. 12, num. 332 and then selects chroma C of fig. 12, num. 322 and then selects luma Y of fig. 12, num. 325 via a "time-division[ ]" in col. 13, lines 37,38 method.).

Yasuki et al. does not teach the limitation of a second circuit configured to generate one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals [that was previously vertically scaled].

On the other hand, Cahill, III et al. discloses an apparatus for variably scaling video picture signals comprising:

a) a first circuit and means (fig. 4,num. 108a-108c: VERTICAL SCALER) configured to generate one or more data signals vertically scaled to a first value (Outputs of fig. 4,numerals 108a-108c.) in response to said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "ILB0") and one or more first control signals (fig. 4, num. 1 18: DISPLAY CONTROL UNIT outputs a control signal to fig. 4,num. 108a-108c: VERTICAL SCALER.);

b) a second circuit and means (Fig. 4,num. 110a-1 10c: HORIZONTAL SCALER) configured to generate one or more output signals horizontally scaled to a second value (Output of figure 4,numerals 110a-110c.) in response (The outputs of fig. 4,numerals 108a-108c are inputted to figure 4,num. 110a-110c via numeral 109 to generate an output of figure 4,numerals 110a-110c in response to the signals of fig. 4,numerals 108a-108c.) to

(i) said one or more data signals (Outputs of fig. 4,numerals 108a-108c.) and

(ii) said one or more first control signals (fig. 4, num. 1 18: DISPLAY CONTROL UNIT outputs a control signal to fig. 4,num. 108a-108c: VERTICAL SCALER and 110a-110c: HORIZONTAL SCALER.), wherein said first value (Outputs of fig. 4,numerals 108a-108c.) and said second value (Output of figure 4,numerals 110a-1 10c.) are independently selectable (Cahill states, "With respect to vertical scaler 108 and horizontal scaler 110, scaling can be...independently programmable in both vertical and horizontal dimensions...(col. 9, lines 21-24)."); and

c) an address generator circuit and means (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) configured to generate said one or more first control signals (fig. 4 or fig. 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 116 and outputs a control signal or "VERTICAL WEIGHT" to fig. 4,num. 108a-108c: VERTICAL SCALER.), wherein said address generator (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) comprises:

c1) a finite state machine (fig. 6A, num.262:ADVANCE STATE MACHINE is contained in figure 5, num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT) configured to allow multiple luma and multiple chroma picture requests to follow in sequence (fig. 6A, num.262:ADVANCE STATE MACHINE is contained in figure 5, num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT that is configured to allow multiple luma picture requests to follow in sequence.).

Cahill, III et al. does not teach the limitation of a finite state machine configured to allow multiple luma and multiple chroma picture requests to follow in sequence.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Yasuki et al.'s teaching of a second circuit (Fig. 12, num. 334 is a second circuit.) configured to generate one or more output signals (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335.) vertically scaled to a second value (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 vertically scaled to a second value using fig. 12, num. 464: VERTICAL PROCESSING SECTION.) in response to said one or more data signals (Fig. 12, num. 334 is a second circuit configured to generate one output signal between numerals 334 and 335 vertically scaled to a second value using fig. 12, num. 464: VERTICAL PROCESSING SECTION in response to said data signals as represented as an arrow outputted from fig. 12,num. 332 and inputted into fig. 12,num. 459 which is inputted to fig. 12,num. 334.) that was previously horizontally scaled with Cahill, III et al.'s teaching of the limitations in paragraphs a and b, because both techniques of either horizontal then vertical scaling or vertical then horizontal scaling can be performed to one of ordinary skill in the art as disclosed in Yasuki et al. and Cahill, III et al., respectively, to achieve the same result of an image that is scaled regardless of the order of operations of vertical or horizontal scaling.

Claims 15 and 16 are rejected the same as claim 1. Thus, argument similar to that presented above for claim 1 of an apparatus is equally applicable to claims 15 of an apparatus with means for limitations and 16 of a method.

Regarding claim 2, Cahill, III et al. discloses the apparatus according to claim 1 wherein said first circuit comprises:

(i) a luma circuit (Fig. 4,num. 102a: Y MEMORY) configured to generate a luma component (Fig. 4, num. 102a: Y MEMORY generates a luma or "Y" component.) of said data signals (Outputs of fig. 4,numerals 108a-108c includes a luma component 108 that originated from fig. 4, num. 102a: Y MEMORY.); and

(ii) a chroma circuit (Fig. 4, num. 102b: U MEMORY and 102c:V MEMORY have the same features as fig. 4, num. 102a: Y MEMORY, thus this limitation is addressed above using fig. 4, num. 102a: Y MEMORY and the respective components to numerals 102b and 102c.) configured to generate one or more chroma components of said data signals (Outputs of fig. 4,numerals 108a-108c.).

Regarding claim 4, Cahill, 111 et al. discloses the apparatus according to claim 1, wherein said apparatus is programmable (Cahill states, "With respect to vertical scaler 108 and horizontal scaler 110, scaling can be... independently programmable in both vertical and horizontal dimensions...(col. 9, lines 21-24).") to scale said output signals (Output of figure 4,numerals 110a-1 10c.) to one or more display modes (fig. 3, num. 1000: VIDEO SYSTEM "supports various modes of operation...(col. 7, lines 46-48).").

Regarding claim 5, Cahill, 111 et al. discloses the apparatus according to claim 4 wherein said apparatus is configured to automatically reset a staring address (fig. 25, num. 1410: READ ADDRESS 720+724 has an address labeled "T12" that is reset at time "T3" of a READ STOBE 1408 of figure 25.) of a display line (A0 of figure 23 is a line of data P0, P2....) when an end (Fig. 25, num. 1404: W1 ACTIVE corresponds to the display line A0 and the address labeled "T12" that does not contain an end of display line because it contains only the first two data 0 and 1 of display line A0 while fig. 25,num 1406: W2 ACTIVE does contain the end 1119" of a display line A0 in col. 24, lines 12-14.) of said display line (Fig. 23, label A0.) is not displayed (Thus, fig. 25,num. 1404: W1 ACTIVE does not display the end 6'19" of display line A0. On the other hand, fig. 25, num.1406: W2 ACTIVE does display the end of display line "19".).

Regarding claim 6, Cahill, 111 et al. discloses the apparatus according to claim 4, wherein said one or more output signals are scalable (Output of figure 4,numerals 110a-110c are scaled values.) to any value in a range of 0.25 times to 4.0 times (A range from 4:1 to 2:1 in col. 20, lines 53-55.) said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0").

Regarding claim 7, Cahill, III et al. discloses the apparatus according to claim 2, wherein said luma circuit comprises:

a) a first memory circuit (fig. 4,num. 107: VERT. PREFETCH BUFFER) configured to buffer a luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are)luma components.) of said video picture signals (fig. 4,num. 104a-104c: "LB1"-and num. 106a-106c: "LB0");

b) a first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR filters in col. 7, line 51.) coupled to said first memory circuit (via figure 3 numerals 1009,1030 and figure 4, label "FROM DMA 1030" of figure 3 and num. 102.) and configured to generate said luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are luma components.) of said data signals (Outputs of fig. 4,numerals 108a-108c.); and

c) a second memory circuit (Fig. 4, num. 109: HORIZ. PREFETGH BUFFER 109.) coupled (via figure 3 numerals 1009,1030 and figure 4, label "FROM DMA 1030" of figure 3 and num. 102,107 and 108.) to said first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR) and configured to buffer said luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are luma components.) of said data signals (Outputs of fig. 4, numerals 108a-108c.).

Claim 8 has the same features of claim 7 except for requiring a chroma circuit as disclosed by Cahill, III et al. in figure 4, numerals 102b and 102c with the same features of a luma circuit of claim 7 and a second filter circuit in figure 3,num. 1022 performs a filtering.

Regarding claim 9, Cahill, III et al. discloses the apparatus according to claim 1, wherein said generator circuit (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) is configured to generate said control signals (fig. 4 or fig, 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 116 and outputs a control signal or "VERTICAL WEIGHT" to fig. 4, num. 108a-108c: VERTICAL SCALER.) in response to one or more second control signals (Figure 5, label: "FROM RASTER CONTROL UNIT 1040") from a microcontroller circuit (fig. 3, num. 1040: RASTER CONTROL UNIT).

Regarding claim 10, Cahill, 111 et al. discloses the apparatus according to claim 9, wherein said apparatus comprises a single-chip MPEG-Z decoder (Fig. 3,num. 1022: VIDEO PROCESSOR includes a decoder in col. 7, line 51.).

Regarding claim 11, Cahill, III et al. discloses the apparatus according to claim 7, wherein said first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR filters in col. 7, line 51.) further comprises:

a) one or more accumulator circuits (Fig. 5,num. 1 16: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT is an accumulator as mentioned in col. 8, line 57,58.) configured to define a number (fig. 5, num. 116 counts with a counter unit.) of said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0") be buffered in said first memory circuit (fig. 4,num. 107: VERT. PREFETCH BUFFER) in response to said one or more first control signals (fig. 4 or fig. 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 1 16 and outputs a control signal to "VERT. PREFETCH BUFFER 107 via control signals "[M]UX SELECT" and "VERTICAL WEIGHT" to fig. 4,num. 108a-108c: VERTICAL SCALER.).

Claim 12 is has the same features as claim 11 except for requiring more of the same components. Thus, claim 12 was addressed in claims 8 and 11.

Regarding claim 13, Cahill, 111 et al. discloses the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 110a-1 10c: HORIZONTAL SCALER) controls an output rate (Fig. 4,num. 110a-110c: HORIZONTAL SCALER outputs a "processing rate" in col. 3, lines 13-16 regardless of slower components in col. 2, lines 57-67.) of said data signals (Outputs of fig. 4,nûmerals 108a-108c.) from said first circuit (fig. 4,num. 108a-108c: VERTICAL SCALER) in response to said first value (Outputs of fig. 4,numerals 108a-108c.) and said second value (Output of figure 4,numerals 110a-110c.).

Regarding claim 14, Cahill, III et al. discloses the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 1 10a-1 10c: HORIZONTAL SCALER) comprises:

a) (via signal "HORIZONTAL WEIGHT" of figure 5.) one or more accumulator circuits (Fig. 5,num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT is an accumulator as mentioned in col. 8, line 57,58.) configured to select one (Fig. 5,num. 1 16 is configured via a "IMIUX SELECT" signal to select data from a buffer 107 to be outputted from VERTICAL SCALER 108 of fig. 5.) or more of said data signals (Output of fig. 5,num. 108: VERTICAL SCALER or outputs of fig. 4,numerals 108a-108c.) in response to said one or more first control signals (fig. 4, num. 118: DISPLAY CONTROL UNIT outputs a control signal or signals "VERTICAL WEIGHT" and "[M]UX SELECT" to fig. 4,num. 108a-108c: VERTICAL SCALER and VERT. PREFETCH BUFFER 107, respectively.).

Claim 18 is rejected the same as claim 13. Thus, argument similar to that presented above for claim 13 is equally applicable to claim 18.

Claim 19 is rejected the same as claim 4. Thus, argument similar to that presented above for claim 4 is equally applicable to claim 19.

Claim 20 is rejected the same as claim 5. Thus, argument similar to that presented above for claim 5 is equally applicable to claim 20.

Regarding claim 21, the combination of Yasuki teaches the apparatus according to claim 1, wherein said finite state machine (Fig. 5, num. 385: STATE MACHINE) comprises:

a) an idle after chroma state (Fig. 12, numeral 459 is a switch is a idle after chroma state when the switch leaves terminal of numeral 369 during selection of a chroma signal ,C of numeral 451 and moves to terminal of numeral 457.) configured to move to any of (i) a luma state (Fig. 12, numeral 459 is a switch is a idle after chroma state when the switch leaves terminal of numeral 369 during selection of a chroma signal ,C of numeral 451 and moves to terminal of numeral 457 to move to a luma state, Y of numeral. 452.), (ii) a BTMP after luma state, (iii) an SPU/VBI state, (iv) an idle after luma state, and a chroma state (Fig. 12, numeral 459 is a switch is a idle after chroma state when the switch leaves terminal of numeral 369 during selection of a chroma signal ,C of numeral 451 and moves to terminal of numeral 457 to move to a luma state, Y of numeral. 452 and a chroma state, C of numeral 452.).

Claim 22 is rejected the same as claim 21. Thus, argument similar to that presented above for claim 21 is equally applicable to claim 22.

Regarding claim 23, Yasuki et al. discloses the apparatus according to claim 1, wherein said finite state machine provides:

(i) an idle after chroma state configured to move to a chroma state (Fig. 12, numeral 459 is a switch is a idle after chroma state when the switch leaves terminal of numeral 369 during selection of a chroma signal ,C of numeral 451 and moves to terminal of numeral 457 to move to a chroma state, C of numeral. 452.)...

... in response to a first predetermined condition state (Fig. 12, numeral 459 is a switch is a idle after chroma state when the switch leaves terminal of numeral 369 during selection of a chroma signal ,C of numeral 451 and moves to terminal of numeral 457 to move to a chroma state, C of numeral. 452 in response to a first predetermined condition state or "empty state" in col. 7, line 55 for FIFO MEMORY 369 of fig. 12.) and

(ii) an idle after luma state configured to move a luma state (Fig. 12, numeral 459 is a switch is a idle after luma state when the switch leaves terminal of numeral 369 during selection of a luma signal ,Y of numeral 451 and moves to terminal of numeral 457 to move to a luma state, Y of numeral. 452.) in response to a second predetermined condition (or "empty state" in col. 7, line 55 for FIFO MEMORY 457 of fig. 12.).

5. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yasuki et al. (US Patent 5,712,689 A) in view of Cahill, III et al. (US Patent 5,784,047 A) as applied to claims 1,15 and 16 above, and further in view of Malinowski et al. (US Patent 5,574,572 A).

Regarding claim 3, the combination of Cahill, III et al. teaches the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 110a-110c: HORIZONTAL SCALER) is further configured to interpolate ("interpolation" in col. 3, line 14) said data signals (Outputs of fig. 4,numerals 108a-108c.).

Cahill, III et al. does not disclose decimation; however, Cahill, III et al. does suggest that "different scaling factor can be used" in col. 20, line 55. Thus, a scaling factor for decimating or shrinking or for interpolating or enlarging a data signal by scaling is suggested by Cahill, 111 et al.

However, Malinowski et al. does teach a use of an "Interpolator" in col. 3, line 40 to col. 4, line 52 and a "Decimating Filter" from col. 4, line 53 to col. 6, line 10 for scaling in col. 3, lines 25-39 as suggested by Cahill, 111 et al.

It would have been obvious at the time the invention was made to one of ordinary skill in the ad to modify Cahill, 111 et al.'s teaching of interpolating with scaling with Malinowski et al.'s teaching of the decimating filter, because, Malinowski et al.'s decimating filter provides "a high quality scaled image (Malinowski et al. col. 2, lines 15-1 9)."

Claim 17 are rejected the same as claim 3. Thus, argument similar to that presented above for claim 3 is equally applicable to claim 17.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario whose telephone number is (571) 272-7397. The examiner can normally be reached on 6-3.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on (571) 272-7695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DR

Dennis Rosario
Unit 2621

JOSEPH MANCUS
PRIMARY EXAMIN